International Journal of Electronics Communication and Computer Engineering
Volume 5, Issue (4) July, Technovision-2014, ISSN 2249–071X

Technovision-2014: 1st International Conference at SITS, Narhe, Pune on April 5-6, 2014

QPSK Modem using FPGA

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Abstract **– This paper presents the basics of QPSK modulation technique. Then the QPSK modulator and demodulator are simulated using Matlab/Simulink environment and System Generator, a tool from Xilinx used for FPGA design. The modulator algorithm has been simulated using Matlab R2011a and System Generator of Xilinx ISE 14.1. This paper describes the functionality of QPSK modem and analyses the performance of QPSK demodulator for AWGN channel. For testing of QPSK modem human speech signal is used as modulating signal.**

Keywords **– QPSK, Simulink, System Generator, FPGA, Xilinx. AWGN.**

I. INTRODUCTION

In QPSK modulation the binary data stream is split into the in-phase and quadrature-phase components. These are then separately modulated onto two orthogonal basis functions, for this two sinusoids are used. Afterwards, the two signals are superimposed, and the resulting signal is the QPSK signal. QPSK system provides double bandwidth compared with BPSK systems.

For QPSK modulations modem chips or ASIC's areused but the systems in which the parameters changes frequently these chips are not suitable as reconfiguration of system and reprogramming is not possible. *FPGA*-Field Programmable Gate Arrays (FPGA) is an *FDP* featuring a general structure that allows very high logic capacity, the most suitable platform in terms of performance, power consumption and configurability. The system based on FPGA has features like reprogrammability and reconfigurability and they are also very easy to upgrade hence it is possible to have flexibility in the product development cycle.

In QPSK data bits to be modulated are grouped into symbols, each containing two bits, and each symbol can take one of four possible values: 00, 01, 10 or 11. During each symbol interval, the modulator shifts the carrier to one of four possible phases 45º, 135º, 225º, and 315ºcorresponding to four possible values of the input symbol. The constellation diagram is shown in figure 1. In QPSK the phase of In-phase (I) cattier is changed from 0º to 180º and Quadrature-phase carrier between 90º and 270º This is used to indicate the four states of a 2-bit binary code. Each state of these carriers is referred to as a Symbol. Two orthogonal carriers are used here one is cos $(2\pi fct)$ and other is sin $(2\pi fct)$, the QPSK signal is represented by

$$s(t) = \frac{1}{\sqrt{2}} dI(t)\cos(2\pi fct) + \frac{1}{\sqrt{2}} dQ(t)\sin(2\pi fct) \quad (2)$$

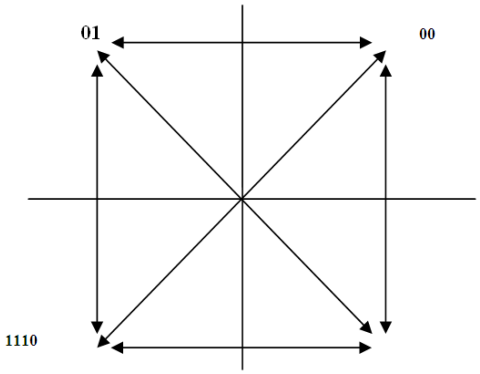

Fig.1. Constellation diagram of QPSK

The rest of paper is organized as: Section II describes the model of QPSK. System design with Simulink models and results are summarised in Section III. Finally the conclusions are presented in Section IV.

II. QPSK MODEM

The block diagram for the proposed work is shown in figure 2.1

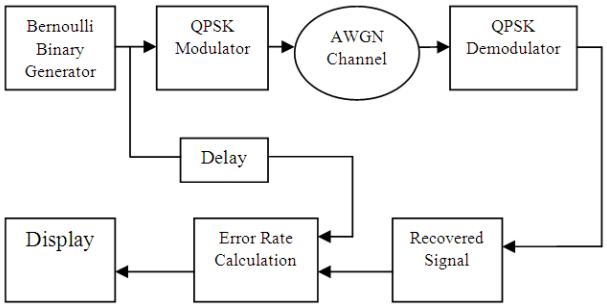

Fig.2.1. Functional Block Diagram of QPSK Modem

The Bernoulli Binary Generator block generates random binary numbers using a Bernoulli distribution. The Bernoulli distribution with parameter p produces zero with probability p and one with probability 1-p.In QPSK there are four phases which are separated by 90^0 data bits to be modulated are grouped into symbols, eachcontaining twobits, and each symbol can take one of four possible values: 00, 01, 10 or 11.In QPSK we can send 2 bits/symbol and so is used for high data-rate applications. Additive white Gaussian noise (AWGN) is a channel model in which the only impairment to communication is

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a linear addition of wideband or white noise with a constant spectral density (expressed as watts per hertz of bandwidth) and a Gaussian distribution of amplitude. The demodulator demodulates the input signal using the binary phase shift keying method. The delay block is used to Sample and hold with one sample period delay. The Error Rate Calculation block compares input data from a transmitter with input data from a receiver. It calculates the error rate as a running statistic, by dividing the total number of unequal pairs of data elements by the total number of input data elements from one source. If the inputs are symbols, then it computes the symbol error rate. Block diagram of QPSK Transmitter and Receiver is as shown in figure 3 and 4 respectively.

A. Transmitter of QPSK

QPSK modulator consists of two binary phase shift keying (BPSK) modulators, the mapping circuit, which is a serial to parallel converter shift register, and carrier generator. The binary serial bit sequence applied to the modulator is converted into two bit parallel sequence of I-bit and Q-bit. These I and Q bits are applied to BPSK modulators whose carrier frequency is orthogonal to each other, which is generated by the carrier generator. The output from both BPSK modulators are then added by summing amplifier which results QPSK modulated signal which can be transmitted by antenna.

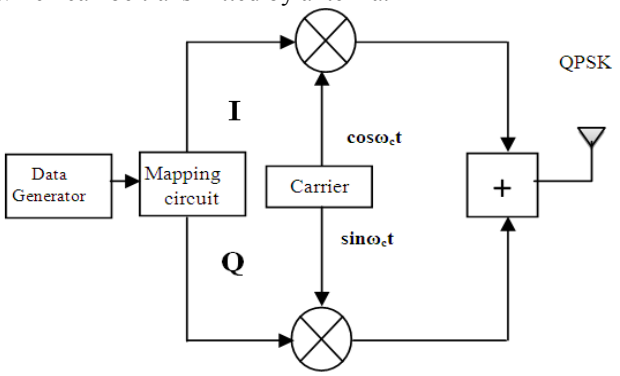

Fig.2.2. Tx of the QPSK [1]

B. Receiver of QPSK

In demodulator the QPSK signal is applied to two balanced modulators and they are multiplied with the same carrier frequency as in the modulator this is called synchronous detection. The output of each balanced modulator contains both baseband components and highfrequency components. The low pass filter removes high frequency components and leaves only baseband components. The filter used is FIR filter. FIR filter is based on frequency characteristics and impulse response. MATLAB's FDA Tool (Filter Design & Analysis) is used to implement FIR filter. Window function design technique is one of the main FIR filter design methods. The basic idea of window function design method is to select the filter on the basis of suitable and ideal frequency characteristics, and then its impulse response is truncated to obtain a FIR filter of linear-phase. The output of two LPF's is then given to the Demapping circuit which gives the original signal m (t).

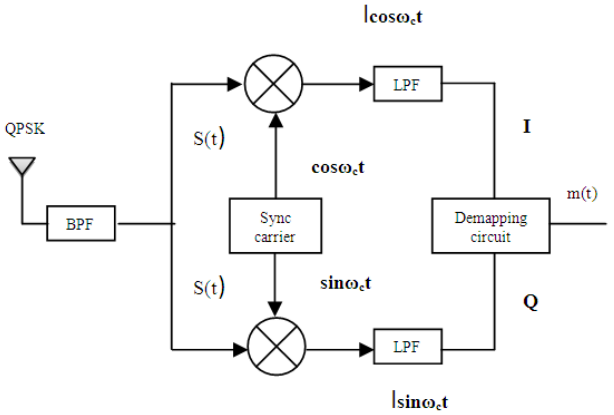

Fig.2.3. Rx of the QPSK [1]

The signal at output of upper balanced modulator is given by following equation.

$$S(t)cos\omega_c t=[\frac{1}{\sqrt{2}}dI(t)\cos\omega_c t+\frac{1}{\sqrt{2}}dQ(t)\sin\omega_c t]\ cos\omega_c t$$

$$=\frac{1}{\sqrt{2}}dI(t)cos^2\omega_c t+\frac{1}{\sqrt{2}}dQ(t)\sin\omega_c t.\ cos\omega_c t$$

$$=\frac{1}{\sqrt{2}}dI(t)[1+\frac{cos2\omega ct}{2}]+dQ(t)\sin\omega_c t\cos\omega_c t$$

$$=dI(t) \quad (3)$$

From equation 3 the In-phase component is obtained. Also the signal at the output of lower balanced modulator is given by,

$$S(t)sin\omega_c t=[\frac{1}{\sqrt{2}}dI(t)\cos\omega_c t+\frac{1}{\sqrt{2}}dQ(t)\sin\omega_c t]\ \sin\omega_c t$$

$$=\frac{1}{\sqrt{2}}dI(t)cos\omega_c t.\ sin\omega_c t+\frac{1}{\sqrt{2}}dQ(t)[1+\frac{sin^2\omega ct}{2}]$$

$$=\frac{1}{\sqrt{2}}dI(t)cos\omega_c t.\ sin\omega_c t+\frac{1}{\sqrt{2}}dQ(t)sin^2\omega_c t$$

$$=dQ(t) \quad (4)$$

Equation 4 shows the Quadrature-phase component. The Demapping circuit adds the I and Q components which results into modulating signal *m (t)*.

III. Simulation using System Generator

Figure 3.1 shows the block diagram of QPSK Modem. In this simulation the recorded voice signal is used as information signal. The information signal is given from the workspace block. This block reads the data file from the workspace. This voice signal is representing the real time application of QPSK modem. Additive White Gaussian Noise (AWGN) channel block is added for linear addition of white noise.

QPSK demodulation using Simulink filter design tool is also shows in figure 3.1. FIR Compiler is used to implement the filters in FPGA. We have to provide the co-

efficient to perform a filtering operation. Here as we need only one type of filter we have used only one FDA module and referenced it in two FIR Compiler modules. This can be done by writing "xlfda_numerator ('FDATool') in co-efficient Vector textbox.

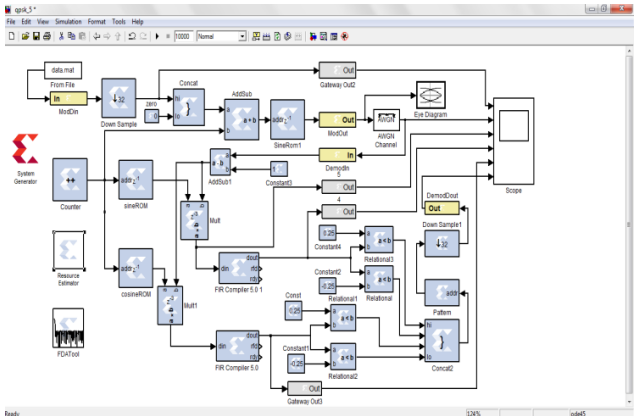

Fig.3.1. QPSK MODEM using System Generator

IV. RESULTS

In this section, simulation model results are based on the Xilinx system generator block set. The following waveform shows the various performance characteristics like eye diagram and simulation of QPSK modulator and demodulator using system generator. The waveforms shows in figure obtained from model shown in figure 3.1. Figure 4.1 represents the information signal from .mat file. Figure 4.2 represents simulation results for QPSK modulator and demodulator.

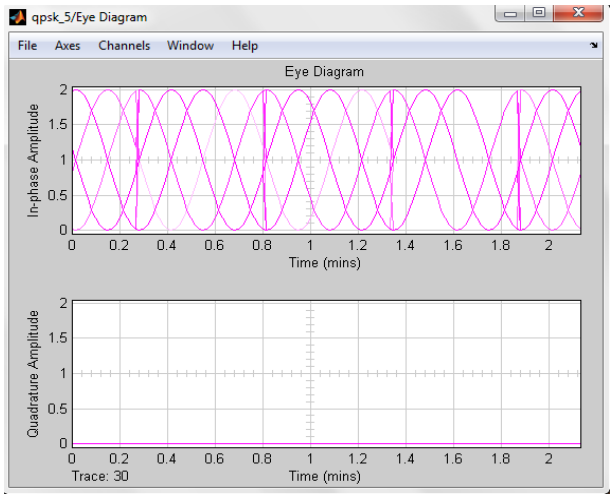

Fig.4.1. QPSK Demodulator using Voice Signal for Binary data

The QPSK modem has a 4MHz clock frequency. Carrier frequency of 125 KHz is obtained as 32 samples are taken for one cycle. The data rate obtained by the design is 250 Kbps. In figure 4.2 the first row shows the data input, second row shows the modulated qpsk signal, third row is the output of multiplier, fourth and fifth row shows the outputs from FIR filters and finally the last row shows the demodulated signal.

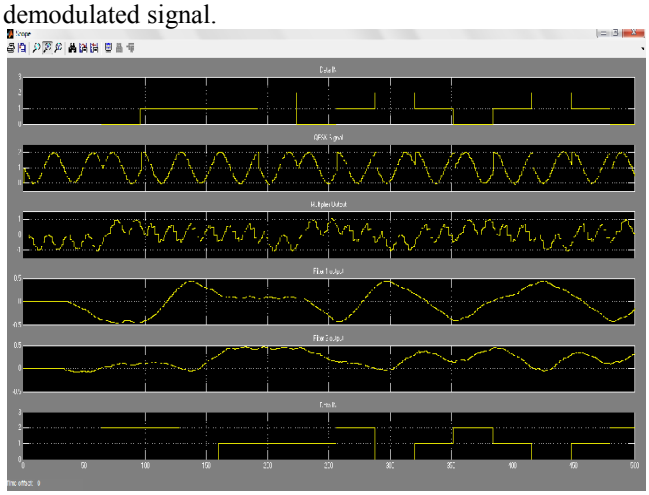

Fig.4.2. Simulation waveforms for QPSK Modem using System Generator

Details of device utilization is discussed in table 1 and corresponding Schematic generated after synthesis is shows in figure 4.3.

Table 1: Design Summary of QPSK Demodulator

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	208	3584	5%
Number of Slice Flip Flops	243	7168	3%
Number of 4 input LUTs	334	7168	4%
Number of bonded IOBs	18	141	12%
Number of GCLKs	1	8	12%

(Target Device- Spartan 3 xc3s400, Xilinx ISE design Suite-14.1)

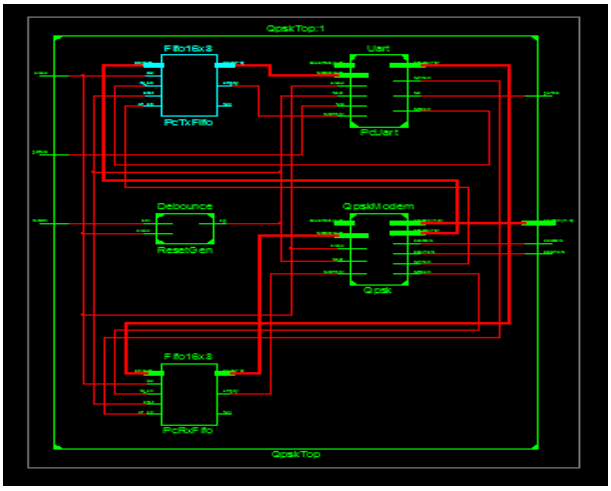

Fig.4.3. RTL Schematic using System Generator

V. CONCLUSION

With this design methodology the typical advantageous features of using field programmable devices are introduced. The design gives the flexibility of reprogramming and reconfiguration. The Simulink simulations are easy to run. These simulations are possible even before the compilation of the System Generator blocks to obtain the hardware description language files. With the System Generator it is possible to simulate the full transceiver, the transmitter and the receiver can be connected through an AWGN channel.

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