International Journal of Electronics Communication and Computer Engineering
Volume 5, Issue (4) July, Technovision-2014, ISSN 2249–071X

Technovision-2014: 1st International Conference at SITS, Narhe, Pune on April 5-6, 2014

BIST Embedding Methodology for Digital Filter

Mayura Thombre
Department of E & TC Engineering
MIT College Of Engineering, Pune
mailto:mayurate@gmail.com

Dr. Mahesh T. Kolte
Department of E & TC Engineering
MIT College Of Engineering, Pune
mailto:mahesh.kolte@mitcoe.edu.in

Mrs. N. S. Warade
Department of E & TC Engineering
MIT College Of Engineering, Pune
mailto:nilima.warade@mitcoe.edu.in

***Abstract* – The test application and area overhead are the two main test parameters is important in digital circuit. If the are is I increased the test time is also increased to minimizing the complexity of and to enhance testability of RTL circuit. BIST embedding methodology is used to overcome this problem. ATPG (automatic test pattern generator) of test application time and BIST area overhead these are two main test parameter which assess the quality of these technique. This methodology is totally different where no duplicate circuitry is required and comparator is checking the response of same type modules external cost is not required. The techniques are suitable for design flow and module are testing using test Register.**

***Keywords* – BIST, Elliptic Filter, FPGA.**

I. INTRODUCTION

In design methodology there are two different technique BIST and ATPG. If we compared the external testing using ATPG this technique is excellent technique. In ATPG technique has three components CUT: circuit under test, it is part which used for manufacturing defects; ATE: Automatic test equipment diagnostics is the part of an ATE test that determines the faulty components complete descriptions of the faulty component. Main function of ATP is to test whether the system is in working condition or not. ATE has following components control processor, timing module, power module and format module; ATP it supplies test patterns and measures test response- but using external testing ATE method. ATPG assess the quality of design for test method they are 1.BIST area over-head 2.performance degradation 3. Test application time 4. Volume of test data 5. Fault-escape probability 6. Efficiency of testable design space exploration. But Automatic test equipment has the following two drawbacks; firstly cost of ATE is extremely expensive. Secondaly if applying scan based DFT test pattern cannot be applied to the circuit under test in a single clock cycle. So they need to be shifted through the scan chain in a scan cycle.

To solve this problem Built in self-test method is used. In BIST method there are two type online BIST and offline BIST. Based on the time of test application and functional operation. BIST is categorized. For functional operation is occurred in online BIST. The advantages of online BIST are to improve fault coverage. On line BIST has excessive power dissipation it reduces reliability and packaging is also increased. For this reason online BIST is inefficient for low power testing. In other case offline BIST is efficient because it dissipate less power as compare to online BIST. The Basic principle of BIST it has TPG and signature analyzer. When the circuit is test mode TPG generator that set. In BIST Technique it employ on chip (TPG)[8]i.e. test pattern generator. When circuit is in test mode TPG set the CUT lines to value that fault free circuit and faulty circuit and signature analyses (SA) evaluates circuit response. It approach for pseudorandom, exhaustive pseudo exhaustive, pseudorandom generation of test pattern is used as LFSR (Linear feedback shift register) as (TPG).LFSR is used for compact and analyses the test responses for single out (CUT).[8]

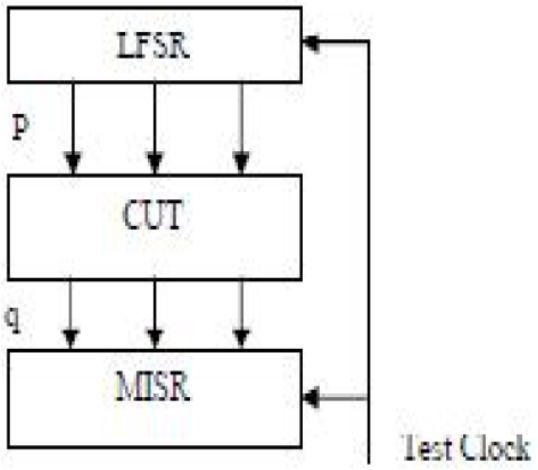


Fig.1. Parallel DIST

Based on tradeoff between test application time required to achieve a satisfactory fault coverage and BIST area overhead associated with extra test hardware. BIST embedding methodology is particular where functional register are modified to test registers to generate test pattern and analyses Test response when the circuit is in the test mode.

The Fig.1 shows BIST embedding methodology. This methodology is parallel BIST embedding methodology. There are three blocks in Parallel BIST LFSR, CUT and MISR. All these three are part of the BIST embedding methodology. In this module for every clock cycle are applied to CUT circuit under test. Which lead to reduction in test application time. In the Fig.1 LFSR [8] for test pattern generator in one entity which is to be tested another entity is MISR for signature analysis a CUT having input and output q.

International Journal of Electronics Communication and Computer Engineering
Volume 5, Issue (4) July, Technovision-2014, ISSN 2249–071X

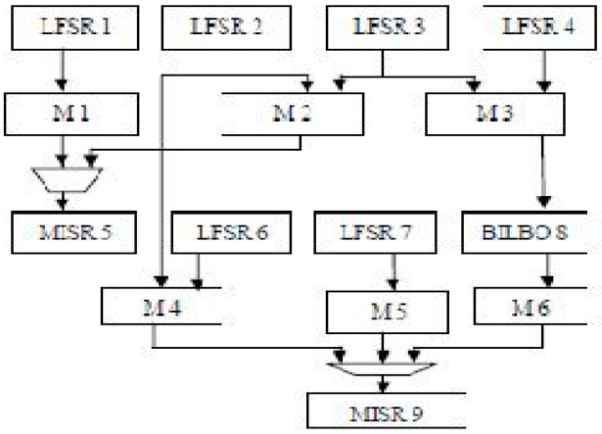
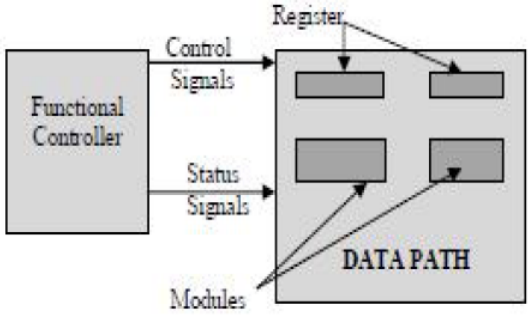


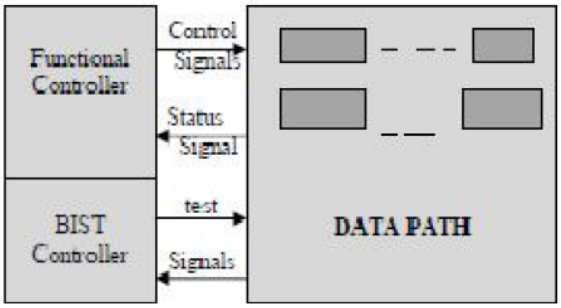
Fig.2. Data Path

II. NEW BIST METHODOLOGY

Another example of BIST embedding methodology for RTL data paths as shown in Fig.2. In data path it consist of six modules R3, R4, R5, R6, R7, R8, and R9 that registers are modified into test register for testing of each input port it is directly or indirectly through the multiplexer fed by a TPG and every output port directly or indirectly feeds a signature analyser In this example M1 LFSR, acts as TPG and MISRs operates as a signature Analyzer. TPG and SA are configured LFSRs, MISRs operates as a signature alanyser.TPG and SA are configured LFSRs, MISRs, BILBOS, [8] & CBILBO. During the test of modules Mk = 1, 2, 3, 4, 5, 6 first initialized the know state test pattern are generated by TPG and applied to Mk from Mk are compressed in signature analyser to form a signature. In this section above section input in test hardware allocated of each module receives test pattern and its output response is observable during test. Test resources to each module are referred to as test synthesis. BIST syntheses are used interchangeably throughout this dissertation. Due to hardware required for TPGS and SAs a BIST data path has a greater area than original circuit. This extra area is BIST area overhead and also test hardware also increases circuit delays so to increase the performance degradation. It is depending on test hardware allocation generated by test synthesis. A test schedule specifies the order of testing all the modules by eliminating all the conflicts between modules.



(a) Functional Data Path



(b) Testable Data Path

Fig.3. Functional and Testable Data Path

In order to achieve minimum area overhead, BIST controller is dividing in functional data path Fig 3(a) to a self testable data path Fig 3(b) with two section functional and BIST controller. The advantage of specifying a system at RTL is to control and status signal during the functional specification are divided and optimized with the test signals that operate the data path during testing. In addition volume of test data: affects storage requirement and shifting time required to shift in the speeds for the TPGS and to shifts out the signatures stored in SAS. So volume of test data has an influence on test application time which is the sum of the shifting time and the time required to complete the test session. High aliasing in signature analysis register leads to data paths with high escape probility which lower fault coverage and hence decreases test efficiency. Finally BIST methodology which asses the quality of BIST are Test application time BIST area overhead, performance degration, volume of test data, fault escape probability, efficiency of teatable design space exploration. So that Test application time (in term of clock cycle) BIST area overhear (in term of square mills).

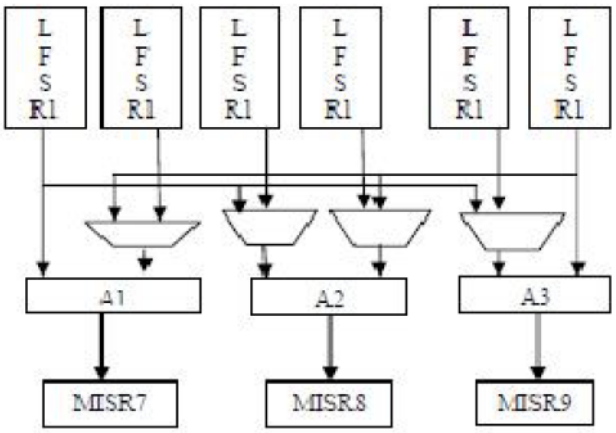


Fig.4. Data Path testing using traditional BIST embedding methodology

Traditional BIST embedding methodology is embedded every module port between a test pattern generator and a signature analyzer register. If the number of test resources

for low test application time is high leading to high BIST area over head and performance degradation. In proposed BIST methodology consider the data path. The data path has 3 module types is A type and register 9.A1-To A3 are the three module. In the test all the modules in a single test session all register are modified into LFSR and MISR. LFSR1 to LFSR6 are applied to test pattern to each input port of module and MISR7-MISR9 is output response of module. The input port is to connect to test pattern generator is through multipliers it is denoted by dotted line. In these modules 2 to 1 mux in data is 4 and hence 24 paths to apply test patterns to module input. To reduce the number of test session in order to reduce BIST area overhead and BIST test application time. LFSR1 is acts as a test register which applies test patterns to left input port of A1, A2, &A3.If mux at left side of port A2 & A3 select LFSR both in BIST area overhead and performance degradation in fig of register R3 & R5 are not modified to performance test function. Similarly A1, A2 selects LFSR6 in fig LFSR3 & LFSR5 are un necessary. LFSR1 and LFSR6 at input of A1 A2 & A3 same test pattern are generated it givens expected at the same time. Hence the output response is checked by CA. MISR& is a signature analysis to detect faults which output response of A1,A2,A3 are equal during test application period but different from the fault free output response of test concurrently solve by three problems. 1. It reduced BIST area overhead (1MISR & 1 comparator vs. 3 MISR) performance degrader (1 MISR vs. 3 MISRs embedded in data paths) 2. IT reduces fault escape probility since faulty output map into fault free signature in the BIST embedding methodology will be detected by compradors'. 3. The number of signatures is reduced by following two application a. Volume of test data in reduced which leads to less storage requirements and test application time in minimized due to less clock cycle reduced to shift out the test response . Given data path width has 8 bits width the time required to shift out the out the output response stored in MISR7,MISR8,&MISR9 is 24 clock cycle. When compared to only 8 clock cycle required to shift out the output response stored in MISR7. Solution using comparator. To enhance built escape probility are based on duplicator form leading to huge BIST area overhead.[4] The proposed methodology is fundamentally different where no duplicate circuitry is required and comparator is checking the responses of same type modules which are instance of same module prototypes. The proposed BIST is suitable for following 1.Complex data path so data flow intensive application domain a. Digital signal processing b. communication c. graphic that have a high number of same type modules generated automatically by modern CAD tools.[2]

The goal of this proposed methodology is to test all the module of the data path which is random pattern resistant and present testability problem. There for the proposed BIST methodology is used to or targeting design a few predesigned module to identical physical and structural details and exploits the data path. The proposed techniques were integrated into VLST design flow by using the (EDA) tools. This experiment is mapping into following data flow.

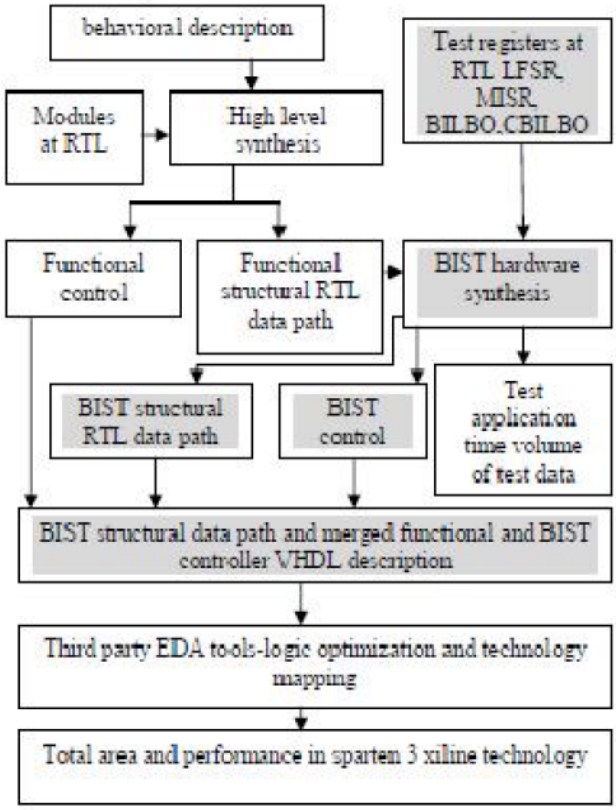


Fig.6. Area and performance estimation for BIST RTL data flow

III. Experimental Validation Flow

In the above Fig. 6 the experimental design flow that developed for purpose of third party tools are shown in shaded box. The Elliptical wave filter, are functional control. The output of high level synthesis is functional control and functional structural RTL data path. BIST hardware synthesis output is BIST control and test application time volume of test data and BIST structural data path. The functional control, BIST controller and BIST structural data path are specified in VHDL and Technology mapping using third party EDA tools in Spartan 3 technology. The results obtained After technology mapping provide total area and performance. The BIST area overhead (BAO), performance, test application time (TAT) using the above experimental figure 6. Thus It should be noted that BIST area overhead includes not only the overhead caused by data path test register, but also the overhead caused by merged functional and BIST controller as shown in Fig. 3 (a),(b)

REFERENCES

[1] Model Technology. *ModelSim Tutorial*. Model Technology Incorporated, 2000.

[2] N. Nicolici and B.M. Al-Hashimi. Power minimization techniques for *Electronics and Photonics* (PREP 2000), 2000 testing low power VLSI circuit *In Postgraduate Research in Electronics and Photonics* (PREP 2000), 2000

[3] H.-C. Tsai, K.-T. Cheng, and S. Bhawmik. On improving test quality of scan based BIST.IEEE *Transactions on Computer-Aided Design of* Integrated Circuits and Systems, 19(8):928– 938 August 2000

[4] V.D. Agrawal, C.-J. Lin, P.W. Rutkowski, S. Wu, and Y. Zorian.Built-in self-test for digital integrated circuits. AT&T *Technical Journal, pages* 30–39, March 1994.

[5] V.D. Agrawal. Editorial - special issue on partial scan design *Journal of Electronic Testing: Theory and Application.*(JETTA), 7(5):5–6, August 1995

[6] V.D. Agrawal, C.R. Kime, and K.K. Saluja. A tutorial on built - in self test - part 1: application IEEE *Design and Test of Computers*,10(1):69-77, June 1993.

[7] V.D. Agrawal, C.R. Kime, and K.K. Saluja. A tutorial on builtin self test - part II: applications IEEE *Design and Test of Computers*,10(1):69-77, June 1993.

[8] M. Serra, T. Slater, J.C. Muzio, and M. Miller. The analysis of one-dimensional linear cellular automata and their aliasing properties. *IEEE Transactions on computer Aided Design of Integrated Circuits and* Systems, , 9(7):767–778, July 1990 Parulkar. *Optimization of BIST Resources During High-Level Synthesis* . PhD thesis, University of Southern California, May 1998.

[9] P. Kollig and B.M. Al-Hashimi. A new approach to simultaneous scheduling, allocation and binding in high level synthesis. *IEE Electronics Letters,* 33(18):1516–1518,Aug 97