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Hardware Implementation of Image Compression Technique using Wavelet

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***Abstract* – Today in the age of technology the use of digital visual system increasing at tremendous rate for information entertainment and education purpose therefore it has become essential to reduce the cost of image transmission and storage as this application have become increasingly importance we give attention towards image compression major objective of image compression is to represent the image as few bit as possible while preserving level of quality and intelligibility regards for given application. Wavelet based image compression provides substantial improvement in picture quality at higher compression ratio. Over the past few years a variety of powerful and sophisticated wavelet based scheme for image compression have been developed and implemented. Because of the many advantages in the upcoming jpeg-2000 standard are all wavelet based compression algorithms. Discrete wavelet transforms is the most popular transformation technique adopted for image compression. Complexity of DWT is always high due to large number of arithmetic operations. The resulting down-sampled pre filtered image remains a conventional square sample grid, and, thus, it can be compressed and transmitted without any change to current image coding standards and systems. The decoder first decompresses the low-resolution image and then up converts it to the original resolution in a constrained least squares restoration process, using a 2-D piecewise autoregressive model and the knowledge of directional low-pass pre filtering. The proposed compression approach of collaborative adaptive down-sampling and up conversion (CADU) outperforms JPEG 2000 in PSNR measure at low to medium bit rates and achieves superior visual quality, as well.**

***Keywords* – Image Enhancement, Autoregressive Modeling, Compression Standards, Image Restoration, Image Up Conversion, Low Bit-Rate Image Compression, Sampling, Subjective Image Quality.**

I. INTRODUCTION

Technological growth of semiconductor industry has led to unprecedented demand for low power, high speed complex and reliable integrated circuits for medical, defense and consumer applications. Today's electronic equipment comes with user friendly interfaces such as keypads and graphical displays. As images convey more information to a user, it is many of the equipment today have image displays and interfaces. Image storage on these smaller, handled devices is a challenge as they occupy huge storage space; also image transmission requires higher bandwidth. Hence most of the signal processing technologies today has dedicated hardware that act as co-processors to compress and decompress images. In this work, a reliable, high speed, low power DWT-IDWT processor is designed and implemented on FPGA which can be used as a co-processor for image compression and decompression.

The prevailing engineering practice of image/video compression usually starts with a dense 2-D sample grid of pixels. Compression is done by transforming the spatial image signal into a space (e.g., spaces of Fourier or wavelet bases) in which the image has a sparse representation and by entropy coding of transform coefficients. Recently, researchers in the emerging field of compressive sensing introduced a new method called "oversampling followed massive dumping" approach. They showed, quite surprisingly, it is possible, at least theoretically, to obtain compact signal representation by a greatly reduced number of random samples.

This project investigates the problem of compact image representation in an approach of sparse sampling in the spatial domain. The fact that most natural images have an exponentially decaying power spectrum suggests the possibility of interpolation-based compact representation of images. A typical scene contains predominantly smooth regions that can be satisfactorily interpolated from a sparsely sampled low-resolution image. The difficulty is with the reconstruction of high frequency contents. Of particular importance is faithful reconstruction of edges without large phase errors, which is detrimental to perceptual quality of a decoded image. For all these drawbacks, new image compression methodology of collaborative adaptive downsampling and up conversion (CADU).

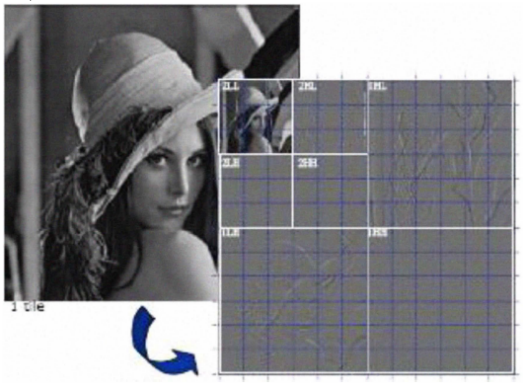


Fig.1. Decomposition of Image [9]

In wavelet transforms, the original signal is divided into frequency resolution and time resolution contents. The decomposition of the image using 2-level DWT is shown in Fig.1 [9, 10, and 11]

II. Discrete Wavelet Transform (DWT)

The Discrete Wavelet Transform, which is based on subband coding, is found to yield a fast computation of Wavelet Transform. It is easy to implement and reduces the computation time and resources required. The discrete wavelet transform uses filter banks for the construction of the multi resolution time-frequency plane. The Discrete Wavelet Transform analyzes the signal at different frequency bands with different resolutions by decomposing the signal into an approximation and detail information. The decomposition of the signal into different frequency bands obtained by successive high pass g[n] and low pass h[n] filtering of the time domain signal. The combination of high pass g[n] and low pass filter h[n] comprise a pair of analyzing filters. The output of each filter contains half the frequency content, but an equal amount of samples as the input signal. The two outputs together contain the same frequency content as the input signal; however the amount of data is doubled.

Therefore down sampling by a factor two, denoted by ↓2, is applied to the outputs of the filters in the analysis bank. The synthesis bank are based on the filters in the analysis bank. Proper choice of the combination of the analyzing filters and synthesizing filters will provide perfect reconstruction. Perfect reconstruction is defined by the output which is generally an estimate of the input, being exactly equal to the input applied. The decomposition process can be iterated with successive approximations being decomposed in return, so that one signal is broken down into many lower resolution components. Decomposition can be performed as ones requirement.

The Two-Dimensional DWT (2D-DWT) is a multi level decomposition technique. It converts images from spatial domain to frequency domain. One-level of wavelet decomposition produces four filtered and sub-sampled images, referred to as sub bands. The sub band image decomposition using wavelet transform has a lot of advantages. Generally, it profits analysis for non-stationary image signal and has high compression rate. And its transform field is represented multi resolution like human's visual system so that can progressively transmit data in low transmission rate line. DWT processes data on a variable time-frequency plane that matches progressively the lower frequency components to coarser time resolutions and the high-frequency components to finer time resolutions, thus achieving a multiresolution analysis. The Discrete Wavelet Transform has become powerful tool in a wide range of applications including image/video processing, numerical analysis and telecommunication. The advantage of DWT over existing transforms, such as discrete Fourier transform (DFT) and DCT, is that the DWT performs a multiresolution analysis of a signal with localization in both time and frequency domain.

A. Proposed Design

The block diagram of the proposed design is shown in fig.2. It consists of a DWT processor and a pair of external dual-port memories. The two memories are initialized with the pixel values of a gray scale image. In this proposed design, input is provided to the DWT processor by importing an image from the workspace in Mat lab. The DWT processor includes DWT filter, memory controller and crossbars. The crossbars are used for interleaving the image pixels i.e. the output of the high pass and low pass filter will be distributed alternatively to the two memory banks.

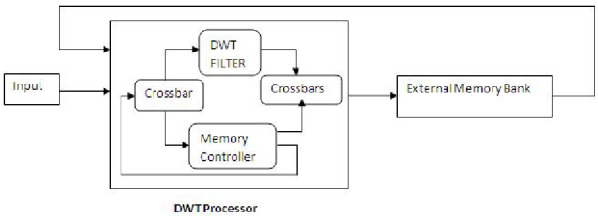


Fig.2. Block diagram of proposed design

The DWT filter is designed using discrete wavelet transform. The Discrete Wavelet Transform can be implemented using high pass and low pass filters. The high pass and low pass filters are designed using following transformations:

$$H(2n+1) = X(2n+1) - floor\left([X(2n) + X(2n+2)]/2\right) \quad (1)$$

$$L(2n) = X(2n) + floor\left([H(2n-1) + H(2n+1) + 2]/4\right) \quad (2)$$

Transformations are performed on each pixel using these filters and this is done as per line basis where lines are defined by start-of-line (sol) and end-of-line (eol). The high pass and low pass filters decompose the image into detail and approximate information respectively. The detail information is basically low scale, high frequency components of the image and it imparts nuance. Whereas the approximate information is high scale, low frequency components of the image and it impart the important part of the image. In the high pass and low pass filter, the new inputs are accepted at one end before previously accepted inputs appear as outputs at the other end. This process is known as pipelining which helps to enhance the speed of the processor. The output of the H and L filters will be alternately distributed to the two memory banks. The data on the 'H' outputs are delayed by 32 cycles relative to the 'L' outputs. Without this delay, the data being written from the 'H' and the 'L' filters would always be trying to write to the same memory bank. With the delay added, they end up always writing to opposite banks.

A memory controller performs the read and writes operation simultaneously. It does not account for latency of getting data from memory or latency of the filter. The

memory control signals are all derived from two free-running counters. The reset holds the counts at zero until a start pulse arrives. The bulk of control is determined on per phase basis from the master counter. The state register defines the number of phases. The address logic is derived by recombination of bits from the master counter for each phase. In fact, the read addresses are just the count value -- i.e. the memory read for this phase is just a stride 1 loop through the whole memory bank. The write addresses for this phase repeat each address twice and given below fig.3.

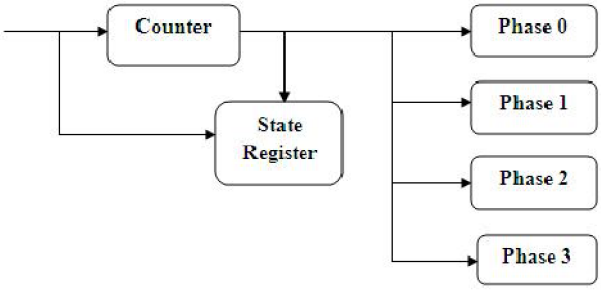


Fig.3. Memory Controller

The external memory bank where the write enable is asserted into variable selector block. The variable selector extracts a subset of rows from the input and fed the output to P1 and P2. These products P1 and P2 perform division and multiplication of its inputs and pass it through write inserter. The write inserter passes first or third input based on the value of second input and output is fed to the read section. This means one word is inserted to the specific address location of external memory bank. And the read section picks up the appropriate word from the memory vector. In case of overlapping of address, the read is done before the write changes the stored word and given below fig.4.

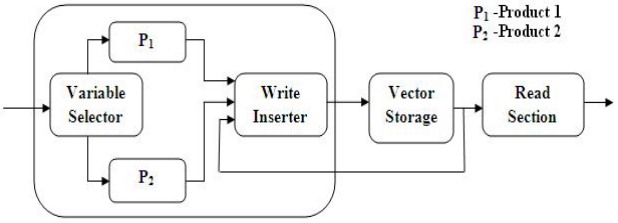


Fig.4. External Memory Bank

III. Implementation of DWT and IDWT Algorithm

In this section we will discuss how to implement 2D FDWT and IDWT together with thresholding in MATLAB. In the FDWT part the input data will be transferred from time domain to scale domain. Then in thresholding part some of the coefficients will be set to zero and in the IDWT part the coefficients will be transferred back into time domain. The block diagram of MATLAB implementation is shown in the fig.5.

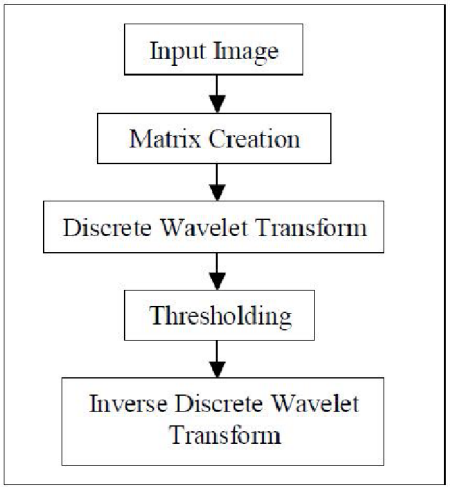


Fig.5. Steps in MATLAB implementation.

While implementing the algorithm in MATLAB the matrix multiplication method has been used. We have tested the[9] as the image input file and also 8 randomly chosen image co-efficient for MATLAB simulation.

After we have achieved satisfactory result in MATLAB we proceed to the next stage where we translate the code into VHDL. The development of algorithm in VHDL is different in some aspects. The main difference is unlike MATLAB, VHDL does not support many built in functions such as convolution, max, mod, flip and many more. So while implementing the algorithm in VHDL, linear equations of FDWT and IDWT is used. The floating point operations have been avoided here. The VHDL code is compiled and simulated using Aldec Active HDL 3.5 software. 8 image coefficient that have been used in MATLAB were also used in VHDL simulation.

Next, the VHDL codes were synthesized using the synthesis tool “Synplify” which have produced “gate level architecture” for VLSI implementation. Finally, the design codes of DWT have been downloaded into FPGA board for verifying the functionality of the design. The simulation results and also the synthesis results are presented.

IV. Introduction to FPGA

FPGA stands for Field Programmable Gate Array which has the array of logic module, I /O module and routing tracks (programmable interconnect). FPGA can be configured by end user to implement specific circuitry. Speed is up to 100 MHz but at present speed is in GHz. Main applications are DSP, FPGA based computers, logic emulation, ASIC and ASSP. FPGA can be programmed mainly on SRAM (Static Random Access Memory). It is Volatile and main advantage of using SRAM programming technology is re-configurability. Issues in FPGA technology are complexity of logic element, clock support, IO support and interconnections (Routing). In this

work, design of a DWT and IDWT is made using Verilog HDL and is synthesized on FPGA family of Spartan 3E through XILINX ISE Tool. This process includes following:

- Translate
- Map
- Place and Route

A. FPGA Flow

The basic implementation of design on FPGA has the following steps.

- Design Entry
- Logic Optimization
- Technology Mapping
- Placement
- Routing
- Programming Unit
- Configured FPGA

Above shows the basic steps involved in implementation. The initial design entry of may be Verilog HDL, schematic or Boolean expression. The optimization of the Boolean expression will be carried out by considering area or speed.

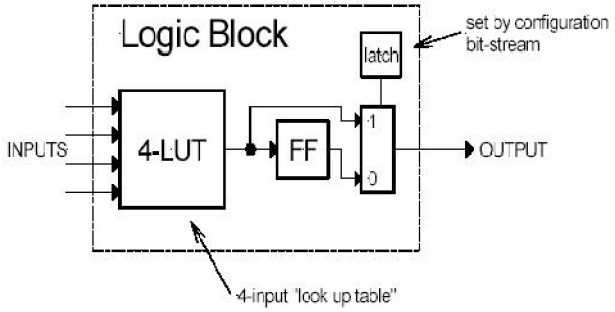


Fig.6. Logic Block

In technology mapping, the transformation of optimized Boolean expression to FPGA logic blocks, that is said to be as Slices. Here area and delay optimization will be taken place. During placement the algorithms are used to place each block in FPGA array. Assigning the FPGA wire segments, which are programmable, to establish connections among FPGA blocks through routing. The configuration of final chip is made in programming unit.

B. Synthesis Result

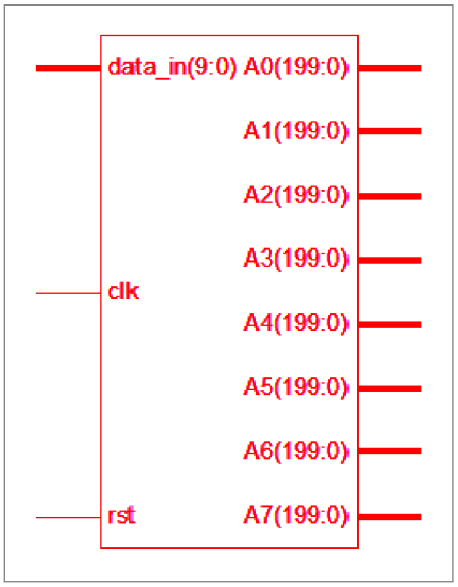
The developed DWT is simulated and verified their functionality. Once the functional verification is done, the RTL model is taken to the synthesis process using the Xilinx ISE tool. In synthesis process, the RTL model will be converted to the gate level net list mapped to a specific technology library. The design of DWT is synthesized and its results were analyzed as follows.

C. DWT Synthesis Result

This device utilization includes the following.

- Logic Utilization
- Logic Distribution

Total Gate count for the Design 3D- DWT Schematic with Basic Inputs and Output



V. Wavelet Domain Image Enhancement

Image denoising and enhancement plays an important role in the field of Image processing. The objective of image enhancement is to improve the visibility of low-contrast features while suppressing the noise. It improves digital quality of image. Image has locally varying statistics, has different edges and smoothness in it. Among various enhancement methods, sharpening techniques are usually designed by using gradient information derived from the Sobel operator, Roberts's operator, or the compass operator. The adaptive enhancement method, exploiting the first derivative, has been used for medical image enhancement [1]. Since differential operators can be regarded as high pass filters, these techniques actually sharpen the image by extrapolation of its high frequency information. The Laplacian pyramid, as one of its variants, has also been used for image enhancement. Image enhancement algorithms generally amplify the noise [2]. Therefore, higher denoising performance is important in obtaining images with high visual quality. Noise reduction can be done on an image by filtering, by wavelet analysis, or by multifractal analysis.

Wavelets are mathematical functions that analyze data according to scale or resolution. It provides a multiresolution representation of continuous and discrete-time signals and images. From their properties and behavior, wavelets play a major role in image compression and image denoising. Among many works about multiscale image analysis, in the pioneering paper [4], an image representation scheme based on multiscale edge decomposition is presented in the context of wavelet theory. Donoho and Johnstone [5] pioneered the work on filtering of additive Gaussian noise using wavelet thresholding. They formalized that effective noise suppression may be achieved by wavelet shrinkage. Given

a set of noisy wavelet coefficients of length and assuming that one has the knowledge of true wavelet coefficients, an ideal filter sets a noisy coefficient to zero if the noise variance is greater than the square of the true wavelet coefficient; otherwise the noisy coefficient is kept. In this way, the mean square error of this ideal estimator is the minimum of variance and the square of the true coefficient. Under the assumption of i.i.d. normal noise, it can be shown that a soft thresholding estimator achieves a risk at most O (log M) times the risk of this ideal estimator.

The wavelet transform provides a scale-based decomposition. The wavelet transform of an image typically Consists of a large number of small coefficients (contain little information) and a small number of large coefficients (contains significant information). Thus each wavelet coefficient is probabilistically in two states: significant and insignificant. For discrete time signals, Discrete wavelet transform (DWT) is implemented by filtering the input signal with a low pass filter and a high pass filter and down sampling the outputs by a factor 2 (Figure 1). Applying the same decomposition to the low pass channel output yields a twolevel wavelet transform; such scheme can be iterated in a dyadic fashion to generate a multilevel decomposition. The synthesis of the signal is obtained with a scheme symmetrical to that of the analysis stage, i.e., by up sampling the coefficients of the decomposition and by low pass and high pass filtering.

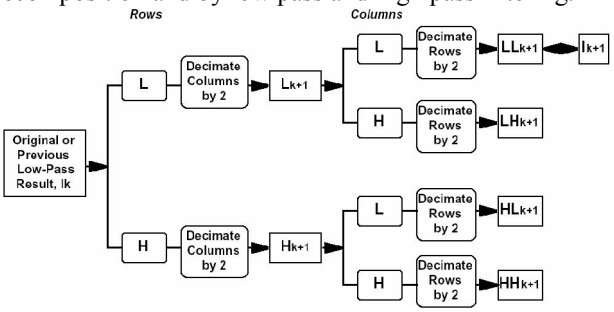


Fig.7. Two dimensional DWT decomposition

VI. Simulation Results

Model Sim simulation results for the proposed design is presented in Fig 8 and Fig 9 for the low pass and high pass filters. Input vectors that were obtained from Mat lab test inputs were used for validating the HDL results. Input vectors are stored in an ROM and are read into the modified DADWT architecture. The decomposed outputs are stored back and are also displayed using simulation waveforms. From the results obtained and compared with Mat lab results it s found that the software and hardware results match and hence validate the functionality of the proposed approach.

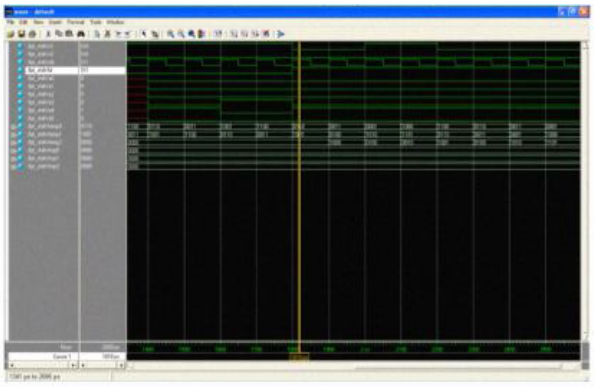


Fig.8. Low pass filter outputs

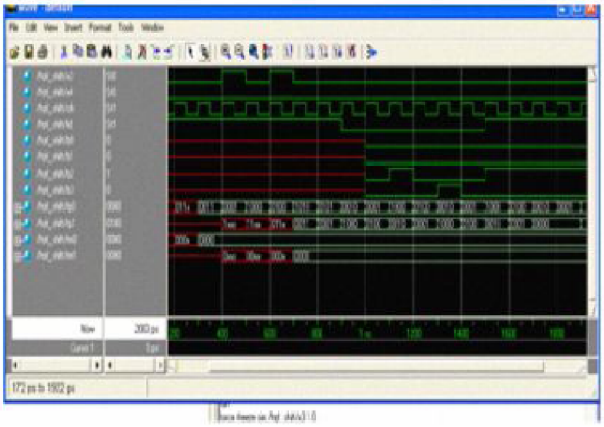


Fig.9. High pass filter outputs

This technique is analyzed using MATLAB software (R2010B). Images are Chaitu.jpg and friend.jpg is Remote sensing image (single band) of 512 x 512 size is taken as an input image. Wavelet transform coefficients are calculated for three scales. Shown below figures is implementation of the denoising algorithm and enhanced algorithm.

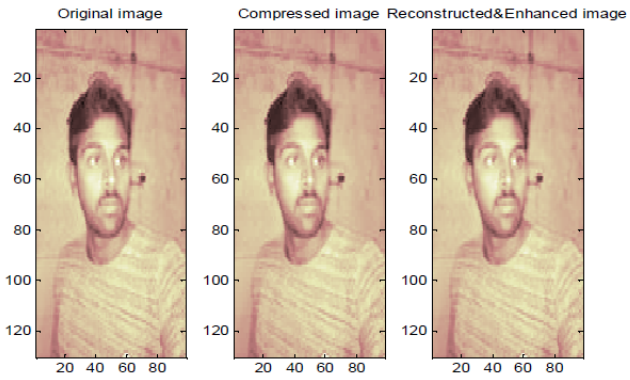


Fig. 10 a) Original Image b) Compressed Image c) Reconstructed and Enhanced Image

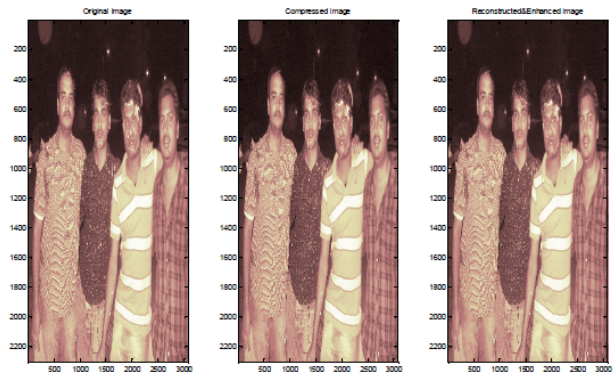


Fig.11. a) Original Image b) Compressed Image c) Reconstructed and Enhanced Image

VII. CONCLUSION

We proposed a new, standard-compliant approach of coding uniformly down-sampled images, which outperforms JPEG 2000 in both PSNR and visual quality at low to modest bit rates. This success is due to the novel up conversion process of least square noncausal predictive decoding, constrained by adaptive directional low-pass prefiltering. Our findings suggest that a lower sampling rate can actually produce higher quality images by multifractal analysis has proved to be the best method. It does a good job in denoising images that are highly irregular and are corrupted with noise that has a complex nature. A wavelet based procedure is used for estimating and controlling the Images. The Discrete Wavelet Transform provides a multiresolution representation of images. The transform has been implemented using filter banks. For the design, based on the constraints the area, power and timing performance were obtained. Based on the application and the constraints imposed, the appropriate architecture can be chosen.

REFERENCES

[1] M. Nagabushanam, Cyril Prasanna Raj p, S. Ramachandran, “Design and FPGA Implementation of Modified Distributive Arithmetic Based DWT – IDWT Processor for Image Compression”, Vo.42, No. 2, pp. 478- 492,2010.

[2] David S.Taubman, Michael W. Marcellin - JPEG 2000 – Image compression, fundamentals, standards and practice", Kluwer academic publishers, Second printing - 2002.

[3] G. Knowles, "VLSI Architecture for the Discrete Wavelet Transform," Electronics Letters, vo1.26, pp. 1184-1185,1990.

[4] M, Vishwanath, R. M. Owens, and M. 1. Irwin, "VLSI Architectures for the Discrete Wavelet Transform," IEEE Trans. Circuits And Systems II, vol. 42, no. 5, pp. 305-316, May. 1995.

[5] AS. Lewis and G. Knowles VLSI Architectures for 2-D Daubechies Wavelet Transform without Multipliers" Electron Letter, vo1.27, pp. 171-173, Jan 1991.

[6] K.K. Parhi and T. Nishitani "VLSI Architecture for Discrete Wavelet Transform", IEEE Trans. VLSI Systems, vol. 1, pp. 191-202, June 1993.

[7] M.Vishwanath, R.M. Owens and MJ. Irwin, "VLSI Architecture for the Discrete Wavelet Transform", IEEE Trans. Circuits and Systems, vol. 42, pp. 305-316, May 1996.

[8] C. Chakrabarti and M. Vishwanath, "Architectures for Wavelet Transforms: A Syrvey", Journal of VLSI Signal Processing, Kulwer, vol.lO, pp. 225-236, 1995.

[9] David S. Tabman and Michael W. Marcelliun, "JPEG 2000 – Image Compression, Fundamentals, Standards and Practice", Kulwer Academic Publishers, Second printing 2002.

[10] Charilaos Christopoulos, Athanassios Skodras, and Touradj Ebrahimi - "THE JPEG2000 STILL IMAGE CODING SYSTEM – AN OVERVIEW", Published in IEEE Transactions on Consumer Electronics, Vol. 46, No. 4, pp. 1103-1127, November 2000.

[11] Majid Rannani and Rajan Joshi, "An Overview of the JPEG2000 Still Image Compression Standard", Signal Processing, Image Communication, vol. 17, pp. 3-48, 2002.

[12] Cyril Prsanna Raj and Citti babu, Pipelined OCT for image compression, SASTech Journal, Vol. 7, pp. 34-38, 2007.

[13] E. Cands, “Compressive sampling,” in Proc. Int. Congr. Mathematics, Madrid, Spain, 2006, pp. 1433–1452. WU et al.: [14] X.Wu,K.U. Barthel, and W. Zhang, “Piecewise 2-D auto regression for predictive image coding,” in Proc. IEEE Int. Conf. Image Processing, Chicago, IL, Oct. 1998, vol. 3, pp. 901–904.

[15] X. Li and M. T. Orchard, “Edge-direted prediction for lossless compression of natural images,” IEEE Trans. Image Process., vol. 10, no. 6, pp. 813–817, Jun. 2001.

[16] D. Santa-Cruz, R. Grosbois, and T. Ebrahimi, “Jpeg 2000 performance evaluation and assessment,” Signal Process.: Image Commun., vol. 1, no. 17, pp. 113–130, 2002.

[17] A.M.Bruckstein, M. Elad, and R. Kimmel, “Downscaling for better transform compression,” IEEE Trans. Image Process., vol. 12, no. 9, pp. 1132–1144, Sep. 2003.

[18] Y. Tsaig, M. Elad, and P. Milanfar, “Variable projection for near-optimal filtering in low bit-rate block coders,” IEEE 160, Jan. 2005.

[19] W. Lin and D. Li, “Adaptive down sampling to improve image compression at low bit rates,” IEEE Trans. Image Process., vol. 15, no. 9, pp. 2513–2521, Sep. 2006.

[20] L. Gan, C. Tu, J. Liang, T. D. Tran , and K.-K. Ma , “Under sampled boundary pre-/post-filters for low bit-rate dctbased coders,” IEEE Trans. Image Process., vol. 16, no. 2, pp. 428–441, Feb. 2007.

[21] X. Zhang, X. Wu, and F. Wu, “Image coding on quincunx lattice with adaptive lifting and interpolation,” in Proc. IEEE Data Compression Conf., Mar. 2007, pp. 193–202.