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VLSI Design and Implementation of Low Power MAC for Digital FIR Filter

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Abstract **- In the majority of digital signal processing (DSP) applications the critical operations are the multiplication and accumulation. Multiplier-Accumulator (MAC) unit that consumes low power is always a key to achieve a high performance digital signal processing system. Finite impulse response (FIR) filters are widely used in various DSP applications .The purpose of this work is to design and implementation of Finite impulse response (FIR) filter using a low power MAC unit with clock gating and pipelining techniques to save power.**

Keywords **- MAC, Low Power, Glitch Reduction, Clock Gating, Latch Based Design, Pipelining.**

I. INTRODUCTION

Finite impulse response (FIR) filters are widely used in various DSP applications .This paper describes an approach to the implementation of low power digital FIR filter based on field programmable gate arrays (FPGAs).The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC for moderate volume applications, and more flexibility than the alternate approaches. Firstly, a single MAC unit is designed, with appropriate geometries that give optimized power, area and delay. Similarly, the N no. of MAC units are designed and controlled for low power using a control logic that enables the each stage at appropriate time. Multiply –Accumulator unit has become one of the essential building blocks in digital signal processing applications such as digital filtering, speech processing, Video coding and cellular phone.

II. MULTIPLY-ACCUMULATE UNITS

A variety of approaches to the implementation of the multiplication and addition portions of the MAC function are possible. A conventional MAC unit consists of multiplier and an accumulator that contains the sum of the previous consecutive products.

The structure of MAC unit is illustrated in Fig.1. It consists of multiplying 2 values, then adding the result to the previously accumulated value, which must then be restored in the registers for future accumulations. The function of the MAC unit is given by the following equation:

$$F = \sum_{i=0}^{N-1} a_i b_i$$

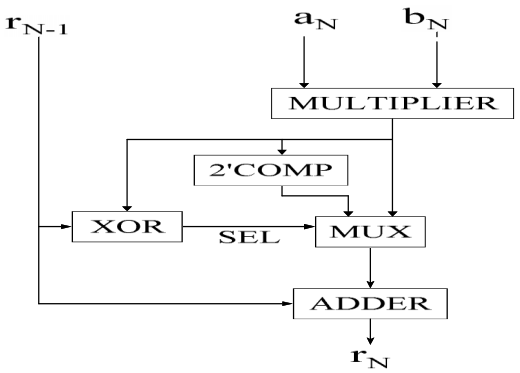


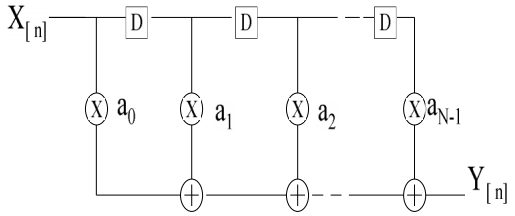
Fig.1. Basic structure of MAC unit

III. FIR FILTERS

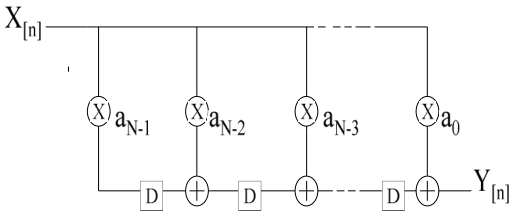
The output of a FIR filter is described by the following equation:

$$y[n] = a_0 x[n] + a_1 x[n-1] + ... + a_{N-1} x[n-N]$$

x[n] is the input signal.y[n] is the output signal. a_i are the filter coefficients, also known as tap weights, that make up the impulse response.The output y of a FIR system is determined by convolving its input signal x with its impulse response a .



(a) Direct form



(b) Transposed form

Fig.2. Various Realizations of FIR Filters

In general, there are two popular forms to realize FIR filters: direct and transposed shown in Fig. 2. In the direct form, there are delay units between multipliers. At a time, the present filter input, x(n), and N-1 previous samples of the input are fed to each multiplier input, and the filter output y(n) is the sum of product of every multiplier. In the transposed form, however, delay units are placed between adders so that the multipliers can be fed simultaneously. For the computation of FIR filter, we have to convolve the input data with filter coefficient, convolution process contains number of multiplication and addition.

IV. Low-Power Designs

Design for low power has become increasingly important in a wide variety of applications, including digital signal processing, mobile computing, high performance computing, and high-speed networking. This section describes various low-power design techniques that can be applied to current FPGA technology. In CMOS circuits, the dominant source of power dissipation is the dynamic power dissipation which is due to the switching of CMOS gates. This includes the clock distribution network consumption and the parasitic power due to glitches.

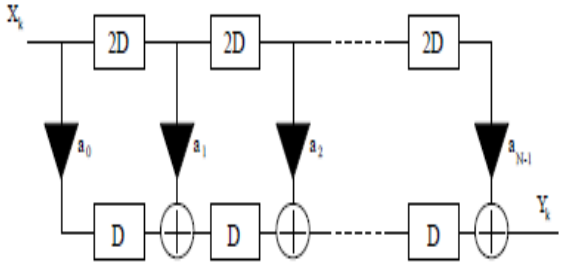


Fig.3. Direct pipe line form of N-tap FIR Filter

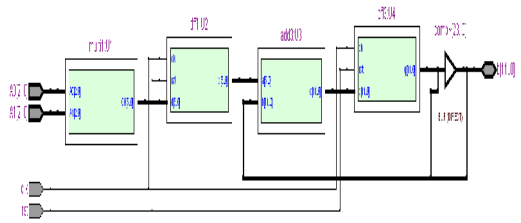


Fig.4. RTL schematic of orignal 4-tap FIR filter

4.1. Glitch Reduction

For arithmetic circuits, a large portion of the dynamic power is wasted on un-productive signal glitches. Glitches are due to converging combinatorial paths with different propagation delays. Signal glitching refers to the transitory switching activity within a circuit as logic values propagate through multiple levels of combinational logic.

4.1.1. Pipelining

Pipelining is a simple and effective way of reducing glitching, and hence minimizing power consumption. It is found that, at a given clock speed, pipelining can reduce the amount of energy per operation by between 40% and 90% for applications such as integer multiplication, CORDIC, triple DES, and FIR filters.

4.1.2. Block-Level Control

We use the XOR tree to select either A or B as the first operand of an adder and C or D as the second operand. Because A, B, C, and D come from registers, they are stable data; but if the control signal of the multiplexers is oscillating, then the operands of the adder are unstable and propagate glitches which consume power .

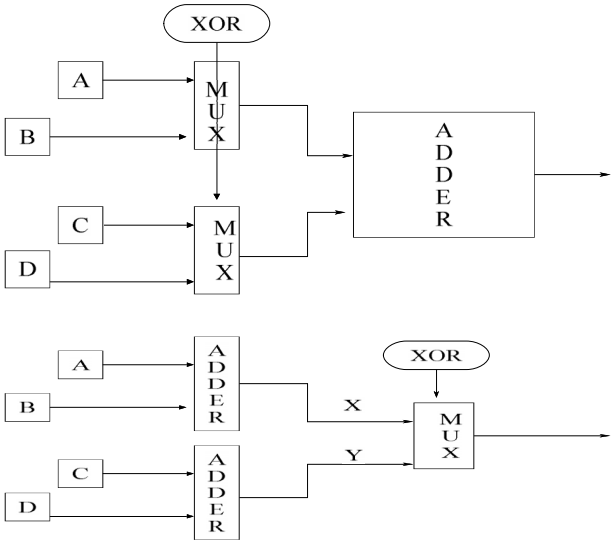


Fig.5. Glitch reduction by block reordering

If we use two adders to compute X and Y sums first and then multiplex them, then adders see stable inputs and have much less power due to glitches shown in fig 3. This reduction comes at the expense of one additional adder block.

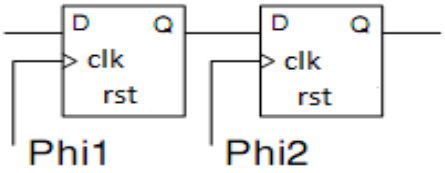


Fig.6. Clock Gating

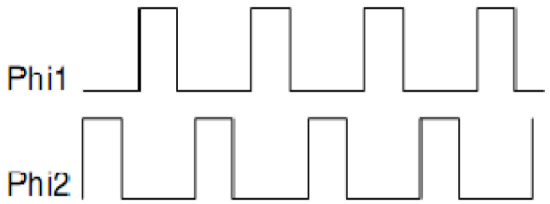


Fig.7. Clock gating Implementation

Clock gating can be used to reduce dynamic power consumption by disabling the clock for the inactive regions to prevent signal transitions. Clock gating (CG) is

illustrated in Fig.4. A block CG, which inhibits the clock signal when the idle condition is true, is associated with each sequential functional unit. The clock signal is computed by function Fcg. CLK is the system clock and CLKG the gated clock of the functional unit. Clock-gating techniques have been successfully implemented in many microprocessors.

Clock gating, which is probably one of the most well-known low-power techniques, is very effective in reducing the power consumption in digital circuits. The goal of this technique is to disable or suppress transitions from propagating to parts of the clock path (i.e., flip-flops, clock network, and logic) under a certain condition computed by clock-gating circuits. The savings are mainly due to the switching capacitance reduction in the clock network and the switching activity in the logic fed by the storage elements because unnecessary transitions are not loaded when the clock is not active.

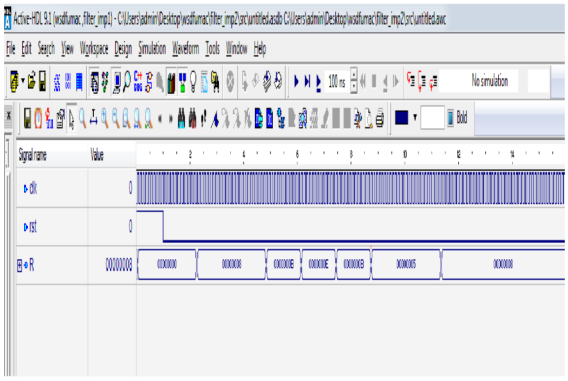


Fig.8. Simulation results for Latch Based 4 tap FIR filter

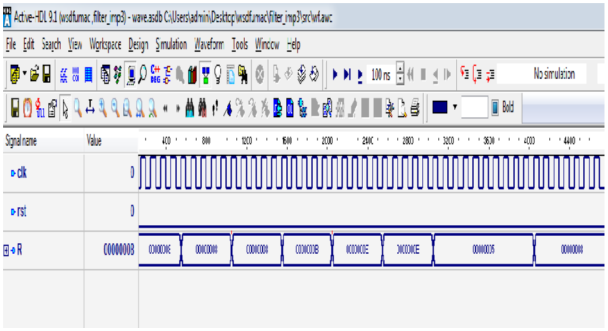


Fig.9. Simulation results for 4 tap pipelined FIR filter

Table 1: 1 Bit Full Adder –Power

Wn/wp	Power(w)	Power(w)
	a=pulse, b=1, cin=0	a=1, b=pulse, cin=o
0.2	3.357 E-10	3.107 E-10
0.3	3.400 E-10	3.797 E-10
0.4	4.430 E-10	4.942 E-10
0.5	3.225 E-10	3.602 E-10

Table 2: 1Bit Full Adder –Delay

Wn/wp	Power(w)	Power(w)
	a=pulse,b=1,cin=0	a=1,b=pulse, cin=o
0.2	4.496 E-10	4.912 E-10
0.3	3.973 E-10	4.317 E-10
0.4	3.663 E-10	3.974 E-10
0.5	3.569 E-10	3.602 E-10

Table 3: Multiplier –Power and Delay

	Power(w)	Delay ‘td’(s)
Wn/wp	i/p=pulse	i/p= pulse
0.2	3.950E-7	9.077 E-09
0.3	1.339 E-9	5.875 E-10
0.4	9.400 E-8	5.511 E-10
0.5	1.379 E-7	5.471 E-10

Table 4: Various Block –Delay, Power, speed and Power Delay product

Blocks	Power (watt)	Delay (s)	Speed (Hz)	Power delay product(fj)
1 bit full adder	0.145n	0.0012n	833.3G	0.000001 74
1 bit D-flip flop	0.0596n	0.01425n	70.17G	0.000008 49
Multi-plier	0.03324u	0.1152n	8.68G	0.0038
MAC unit	0.007698m	0.437n	2.288G	3.364

V. CONCLUSIONS

A VLSI architecture for low power MAC have been presented in this paper. The basic building blocks for the MAC unit are identified and each of the blocks is analyzed for its performance. Power will be calculated for the blocks. 1-bit MAC unit will be designed with enable to reduce the total power consumption based on above proposed techniques. Using this block, the N-bit MAC unit will be constructed and the total power consumption will be calculated for the MAC unit. The dynamic power which is determined by the equation where alpha is the switching activity factor, C is the capacitance, V is the supply voltage, and f is the clock frequency. To achieve low power in circuits one or more of the parameters must be minimized. The MAC unit designed in this work can be used in filter realizations for High speed DSP applications.

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